Reg. No. :

Name :

Third Semester B.Tech. Degree Examination, January 2016 (2013 Scheme) 13.304: ANALOG ELECTRONICS (E)

Time: 3 Hours

Max. Marks: 100

TRIVANDRUM-1

PART-A

Answer all questions briefly. Each question carries 2 marks.

- 1. Why S_l is considered and S_V or S_β not taken into consideration during the design the of an amplifier?
- 2. Why compensation is essential, in addition to the stabilization of an amplifier circuit?
- 3. Compare input resistances of the three configurations of BJT, giving typical values in each case.
- 4. Define pinch off voltage of JFET? List the parameters which control it.
- 5. Define f_T of a BJT? Why it is chosen as the figure of merit?
- 6. Why it is not possible to use the h-parameters at :
 - i) high frequencies and ii) large signals?
- 7. Derive equations to show that the sensitivity of gain is decreased with the application of negative feedback to an amplifier.
- 8. Why voltage series feedback is most commonly used in cascaded amplifiers?
- A peak-to-peak input signal of 0.5 V has to produce a peak-to-peak undistorted output voltage of 3V with a rise time of 4 μ s. Can 741 op-amp be used for this application? Justify.
- 10. Why open loop configurations of op-omp cannot be used for linear applications?

 (10×2=20 Marks)



15

5

10

10

12

8

8

12

PART-B

Answer any one full question from each Module. Each full question carries 20 marks.

Module - I

- 11. a) Define the three stability factors of BJT amplifier. With necessary circuits, derive the expressions for the stability factors for the collector feedback bias circuit. Why this circuit is not preferred practically?
 - b) For the above circuit draw the ac and dc load lines and explain.

OR

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- 12. a) A potential divider bias CE amplifier circuit is used with V_{CC} = 11 volt, R_C = 5.1 K, β = 100, V_{BE} = 0.65 V. It is desired to fix the Q-point (5.5 V, 1mA) with its current stability factor S \leq 15. Draw and design the circuit.
 - b) With necessary circuit and equations, explain the bias compensation against V_{BE} to I_{CO} .

Module - II

- 13. a) With neat constructional diagram, explain the working principle of a JFET? Explain its characteristics and applications.
 - b) Prove that the transconductance g_m of a JFET is $g_m = \frac{2}{|V_p|} \sqrt{I_{DS} I_{DSS}}$.

OR

- 14. a) Draw the circuit diagrams of 2 stage:
 - i) RC coupled
 - ii) Transformer coupled and
 - iii) Emitter coupled DC amplifiers and discuss the important features of each one, bringing out their applications.
 - b) Draw the circuit of a Darlington pair amplifier and derive expressions for its R_i, R_o, R_i and A_v.

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Module - III

15. a) Describe the circuits of series fed and transformer fed class A power amplifier and derive expressions for its efficiency in both cases. 12 b) Class B push-pull amplifier is supplied with $V_{CC} = 50 \text{ V}$. The signal swings the collector voltage down to V_{min} = 10 V. The dissipation in both transistors total 40 W. Calculate the total power and conversion efficiency. Draw the circuit. OR a) Draw the circuit example for a circuit series feedback. Find the feedback factor. Derive its R; and gain with and without feedback. b) Draw the circuit diagram of a crystal oscillator using BJT amplifier and explain how oscillations are started and sustained in it? 8 Module - IV 17. a) Why do offset current and offset voltage exist in an op-amp? What are the various ways of minimising them? Give their typical values for 741. 10 b) What is virtual short? Explain with a circuit example the conditions to be satisfied to have virtual short? What are the errors encountered by considering this concept? 10 OR 18. a) Why regenerative feedback is required in a comparator? Explain with its transfer characteristics, for the circuits with and without regenerative feedback. 8 b) Draw the circuit of an op-amp linear sweep generator, which uses no input signal. With the help of appropriate waveforms, explain its working. Derive equations for the sweep amplitude and frequency. 12 (4×20=80 Marks)